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EXAMINER	
KRAVETS, LEONID	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,315	ZIEVERS, PETER J.	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

1. Acknowledgment is made of the information disclosure statement received April 25, 2005.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters 802, 803, 804 and 902,903, 904 have both been used to designate the same parts in different drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 200, 400, 500, 501, 502, 503, 504, 506, 507, 508, 800 etc. Corrected

drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claim 3 is objected to because of the following informalities: "processes" should be "process". Appropriate correction is required.

2. Claim 13 is objected to because of the following informalities "the" in line 3 should be "to". Appropriate correction is required

3. Claim 16 is objected to because of the following informalities: "be" is mistyped as "by". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 6 recites the limitation "said step of transmitting a read request". There is insufficient antecedent basis for this limitation in the claim. Examiner interprets the limitation to mean "generating a request for reading".

6. Claim 9 recites the limitation "transferring said buffers **from** said bulk memory". There is insufficient antecedent basis for this limitation in the claim. Examiner interprets this claim to depend on claim 2.

7. Claims 14 and 15 recite the limitation "said state controller". There is insufficient antecedent basis for this limitation in the claim. State controller will be interpreted as a controller.

8. Claim 16 recites the limitation "buffering the requests of other buffers". A buffer can be buffered, however a buffer can not request for itself to be buffered. Examiner interprets this to mean "buffering the requests of other high speed memories.

9. Claim 17 recites the limitation "said multiplexer". There is insufficient antecedent basis for this limitation in the claim. Multiplexer will be interpreted as a controller.

10. Claims 18 and 20 recite the limitation "the busy/idle state". There is insufficient antecedent basis for this limitation in the claim. Examiner interprets the signal to be a selector signal identifying a free memory.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Ferguson et al. (US Patent 6,798,777).

13. As per claim 1, Ferguson discloses a method of operating a memory management system adapted to process linked list data files (Col 41, Lines 43-48); said system comprises a plurality of low storage capacity high speed memories [Ferguson describes queues implemented on a per-port basis, thus each port has its own queue and memory (Col 41, Lines 42-46)] and a lower speed high storage capacity bulk memory (Fig 3, Ref 319), said high speed memories have a first data rate, said bulk memory has a second data rate lower than said first data rate, said system further comprises an access flow regulator for generating requests for the reading and writing of linked lists by said memories (Col 41, Lines 31-35), said method comprises the steps of:

initiating the writing of a linked list in said high speed memories by transmitting a write request from said access flow regulator to said high speed memories [Note queue is interpreted as linked-list in this instance, as the queue has pointers, a trait of linked-lists (Col 41, Lines 31-35)];

writing a head buffer and a tail buffer and at least one intermediate buffer of said linked list into said high speed memories (Col 41, Lines 31-35); and

transferring said at least one intermediate buffer from said high speed memories to said bulk memory while leaving the head buffer and the tail buffer in said high speed memories (Col 41, Lines 57-60).

14. As per claim 2, Ferguson discloses a method of operating a memory management system adapted to process linked list data files (Col 41, Lines 43-48); said

system comprises a plurality of low storage capacity high speed memories [Ferguson describes queues implemented on a per-port basis, thus each port has its own queue and memory (Col 41, Lines 42-46) and a lower speed high storage capacity bulk memory (Fig 3, Ref 319), said high speed memories have a first data rate, said bulk memory has a second data rate lower than said first data rate, said system further comprises an access flow regulator for generating requests for the reading and writing of linked lists by said memories (Col 41, Lines 31-35), said method comprises the steps of:

transmitting a read request for a specified linked list from said access flow regulator to said high speed memories containing buffers of said specified linked list (Col 43, Lines 28-30);

reading the head buffer of said specified linked list (Col 43, Lines 20-21);

transferring said at least one intermediate buffer of said linked list from said bulk memory to one of said high speed memories [it is inherent that once a head buffer is read, a new buffer will replace it given that the head buffer is the top of the queue];

designating the intermediate buffer transferred to in said one high speed memory as the replacement head buffer of said specified linked list [Ferguson discloses that the region for a queue can be one cell (Col 43, Lines 10-12), thus if the head is one cell, a new cell replacing the read cell would be designated the head cell];

reading out said intermediate buffer of said specified linked list from said one high speed memory [The intermediate buffer is now the head buffer, thus the method repeats (Col 43, Lines 20-21)]; and

transmitting said read out buffers of said specified linked list to said access flow regulator [Buffer of Ferguson is within the multi-function multi-port along with the output request processor making the read requests, thus they are one unit (Col 44, Lines 8-10)].

15. As per claim 3, Ferguson discloses the method of claim 1 further including the step of operating said system to concurrently process linked lists for a plurality of requests from said access flow regulator [Output switch communicates directly with each output request processor, thus these units are considered one access flow regulator. The output switch transmits to the output request processors of each multi-function multiport (Col 41, Lines 9-11)].

16. As per claim 4, Ferguson discloses the method of claim 1 further including the step of operating said system to process buffers of a linked list stored in different ones of said high speed memories [the linked list queues in each multi-function multiport are independent and thus are processed in different high speed memories (Col 41, Lines 20-26)].

17. As per claim 5, Ferguson discloses the method of claim 1 further including the step of operating said system to write a tail buffer as the first buffer written to a new linked list [Col 42, Lines 6-9)]; and

the step of reading the head buffer of a linked list first (Col 43, Lines 20-21).

18. As per claim 10, Ferguson discloses the method of claim 1 including the further steps of:

writing buffers to an existing linked list by transferring the existing tail of said existing link list from said high speed memories to said bulk memory (Col 42, Lines 9-11); and

writing a new buffer as a new tail buffer of said existing link list in said high speed memories (Col 42, Lines 6-9).

19. As per claim 11, Ferguson discloses the method of claim 1 including the further steps of:

embodying said system into a network node having incoming and outgoing links (Fig 2B);

applying linked list buffers received by said links to said access flow regulator (Fib 2B); and

processing said buffers by said memories to control the data throughput of said network node (Col 41, Lines 31-35).

20. As per claim 19, please see rejection of claims 1 and 2. Claim 19 has a limitation claiming an apparatus for subsequently reading out said head buffer and said tail buffer as well as said intermediate buffers from said high speed memories. The apparatus of

Ferguson reads out head buffers; however, it is noted that with time this would read out all buffers, including intermediate and tail buffers.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. Claims 6-7, 12, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson as applied to claim 1 above, and further in view of Brigati (US Patent 6,279,068).

As per claim 6, Ferguson discloses the method of claim 1 wherein said system further comprises a plurality of state controllers each of which is individual to one of said high speed memories (Fig 3, Ref 306), said system further comprises a request bus

connecting said access flow regulator with said state controllers (Fig 3, Ref 102). Ferguson does not disclose the method wherein said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said read request;

transmitting said read request from said access flow regulator over said request bus to the state controller individual to said selected high speed memory; and

operating said state controller to extend said read request to said selected high speed memory.

Brigati and Ferguson further disclose the method wherein said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said read request (Brigati, Col 2, Lines 24-27; Col 3, Lines 4-8);

transmitting said read request from said access flow regulator over said request bus to the state controller individual to said selected high speed memory [The access flow regulator must transmit to the state controller individual to said selected high speed memory, as in the system of Ferguson only output switch 102 connects each multi-function multiport to the output switch (Fig 3, Ref 102)]; and

Ferguson further discloses operating said state controller to extend said read request to said selected high speed memory (Col 41, Lines 31-35).

As per claim 7, Ferguson and Brigati disclose the method of claim 6 wherein said step of operating said state controller includes the further steps of:

determining the present occupancy level of said selected high speed memory (Ferguson, Col 42, Lines 22-24);

transmitting said request to said high speed memory if said present occupancy level is not exceeded (Ferguson, Col 42, Lines 19-22); and

requesting a connection to said bulk memory if said present occupancy level of said selected high speed memory is exceeded [Since when the occupancy level is exceeded, most cells are stored in bulk memory, a connection to bulk memory must be made to read data that has been moved into this memory from the high speed queue (Ferguson, Col 42, Lines 22-24)].

As per claim 12, Ferguson and Brigati disclose the method of claim 6 wherein said step of operating said state controller includes the further steps of:

concurrently receiving buffers of multiple linked lists [In the system of Ferguson, each state controller (output request processor) of the multi-function multiport receives buffers of linked lists, thus the state controllers are concurrently receiving buffers of multiple linked lists];

separating the buffers of multiple linked lists directed to said access flow regulator [each cell of Ferguson is independent, with a pointer to another cell, thus they are separated (Fig 13)]; and

extending multiple accesses received by said access flow regulator to said high speed memories [all accesses received by access flow regulator are forwarded to the output request processor which in turn processes the requests through the head-tail buffer (high-speed memories) (Col 43, Lines 20-31)].

As per claim 18, Ferguson discloses the method of claim 1. Brigati discloses the method comprising the further steps of:

generating a signal unique to each high speed memory indicating the busy/idle state of each said high speed memory (Paragraph 17);

extending each generated signal to said access flow regulator [The signal must be extended to the access flow regulator for it to be able to make decisions on where to send the data];

operating said access flow regulator to receive requests for the writing or reading of linked lists by said high speed memories (Ferguson, Col 41, Lines 9-11) ;

operating said access flow regulator in response to the receipt of a request to read said busy/idle signals generated by said high speed memories [Brigati discloses using the selection signal to select an idle memory, in the system of Ferguson, this task would be performed by the output processor (Brigati, Paragraph 17)];

operating said access flow regulator to response to said reading to identify an idle one of said high speed memories [In the system of Brigati, the idle memory is the one which is not being written and thus can be selected from the selection signals (Brigati, Paragraph 17)]; and

operating said access flow regulator for extending a request for the reading or writing of a data file [interpreted as linked list] to said idle one high speed memory [Brigati discloses extending a read/write request to the idle memory (Paragraph 11)].

As per claim 20, please see rejections of claims 2 and 18 above. Claim 20 is a combination of these claims.

With regard to claims 6-7, 12, 18 and 20, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the selection of idle memory of Brigati into the system of Ferguson, since Ferguson and Brigati form the same field of endeavor, namely data transfer between memories and this would allow for reads and writes to not have to wait for a busy memory to become idle (Brigati, Paragraph 11).

24. Claims 8 and 16 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Brigati as applied to claim 6 above, and further in view of Lee et al (US PG Pub 2004/0205305).

As per claim 8, Ferguson and Brigati disclose the method of claim 6. They do not disclose the method wherein said system further includes a multiplexer, and an access bus connecting said state controllers with said multiplexer.

Lee discloses such a multiplexer (Fig 1, Ref 54), and an access bus connecting memories to a multiplexer (Fig 1, Ref 50). The system of Lee further includes a bus connecting said multiplexer with said bulk memory; said method includes the further steps of operating said multiplexer to:

Receive a request from said state controllers for a connection to said bulk memory [In the system of Lee, FIFOs request transfer of files to a bulk memory (Fig 1). The system of Ferguson and Brigati would use such a multiplexer to create one bulk memory for all the multi-function multiports and to transfer from each head-tail queue into a common notification memory];

Determine which one of a plurality of requesting state controllers is to be granted access to said bulk memory [A multiplexer selects one input from several possible inputs to output (Fig 1, Ref 54)];

Connect one of said requesting state controllers to said bulk memory [A multiplexer selects one input from several possible inputs to output, thus connecting the FIFO of Lee to the memory]; and control the operation of said bulk memory in the transfer of data from said one high speed memory to said bulk memory [Multiplexer can connect or disconnect any memory, thus it controls the operation of the bulk memory in the transfer of data].

Applying buffers of said linked list from said state controller to said multiplexer via said access bus (Lee, Fig 1, Ref 40-47, 50, 54).

As per claim 16, the method of Ferguson, Brigati and Lee discloses the method of claim 8 wherein said step of operating said multiplexer includes the further steps of:

determining which one of a plurality of bidding high speed memories is to be granted access to said bulk memory [A multiplexer selects one input from several possible inputs to output (Fig 1, Ref 54)]; and

buffering the requests of other buffers in said one high speed memory [Though Lee does not expressly disclose a buffer in the multiplexer, one of ordinary skill in the art would have found it obvious to add such a buffer to the multiplexer in order to free the high speed memories from waiting to transfer to the bulk memory, thus allowing them to perform other such as storing new cells in the head-tail queue of Ferguson].

With regard to claims 8 and 16, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Lee into the system of Ferguson and Brigati, since Ferguson, Brigati and Lee form the same field of endeavor, namely data transfer between memories and this would allow for sharing of a bulk memory between the high-speed memory, providing a cost savings in the system.

25. Claims 9, 14, 15, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson as applied to claim 2 above, and further in view of Milway (US Patent 6,470,428).

As per claim 9, Ferguson discloses the method of claim 2.

Ferguson and Milway further disclose the method wherein said step of transferring said buffers from said bulk memory includes the steps of:

reading out intermediate buffers of a linked list from said bulk memory to said high speed memories in a burst mode having a data rate substantially equal to the data rate of said high speed memories (Milway, Col 1, Lines 59-64);

storing said read out buffers in said high speed memories (Ferguson, Col 42, Lines 9-11); and

subsequently reading out buffers of said linked list from said high speed memories for transfer to said access flow regulator [Buffer of Ferguson is within the multi-function multi-port along with the output request processor making the read requests, thus they are one unit (Ferguson, Col 44, Lines 8-10)].

As per claim 14, Ferguson and Milway disclose the method of claim 9 wherein said step of operating said state controller includes the further steps of:

controlling transfer of a buffer from said high speed memory in a burst mode to said bulk memory [Milway discloses using burst transfers, while Ferguson discloses transferring cells from the head-tail buffer to the notification area (Milway Col 1, Lines 59-64; Ferguson Col 42, Lines 22-24). While the system of Milway transfers data in bursts from memory to cache, a person of ordinary skill in the art would understand that the opposite transfer would serve the same purpose of speeding up memory transfers]; and

controlling transfer of a buffer from said bulk memory to said high speed memory (Ferguson, Col 42, Lines 6-11) .

As per claim 15, Ferguson and Milway disclose the method of claim 14 wherein said step of operating said state controller includes the further steps of:

determining whether said bulk memory is idle when a transfer is requested;

extending said buffers to said bulk memory if idle; and

buffering said transfer if said bulk memory is busy.

[It would have been obvious to one of ordinary skill in the art to transfer a buffer to bulk memory if the bulk memory is idle or to buffer the transfer if it is busy for later transfer].

As per claim 17, Ferguson and Milway disclose the method of claim 9 wherein said step of operating said multiplexer includes the further steps of:

determining the identity to the high speed memory to which a buffer is to be directed from said bulk memory [In the system of Ferguson, each multi-function multiport is unique, thus each high speed memory (head tail queue) is unique and is identified as such]; and

controlling the transfer of said buffer in a burst mode from said bulk memory to said identified high speed memory (Milway, Col 1, Lines 59-64).

With regard to claims 9, 14-15 and 17, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the burst

transfer of Milway into the system of Ferguson, since Ferguson and Milway form the same field of endeavor, namely multi tiered memory hierarchies and this would allow for faster transfer of data between the storage and memory by transferring several data units at once (Milway, Col 1, Lines 61 63).

26. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson in view of Brigati as applied to claim 6 above, and further in view of Klikki (US Patent 6,868,061).

As per claim 13, Ferguson and Brigati disclose the method of claim 6 wherein said step of operating said state controller includes the further steps of:

responding the each received request to determine the present occupancy level of the high speed memory individual to said state controller (Col 6, Lines 51-54);

extending said access to said associated high speed memory if said present occupancy level is not exceeded (Col 7, Lines 49-53); and

signaling said access flow regulator to buffer said request if said present occupancy level is exceeded [The system of Klikki discards cells once the occupancy level threshold is exceeded, however, one of ordinary skill in the art would understand that instituting a buffer for these cells would allow for less dropped packets and thus better network reliability (Col 7, Lines 45-49)].

With regard to claim 17, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the occupancy level of Klikki into the system of Ferguson and Brigati, since Ferguson, Brigati and Klikki form the same field of endeavor, namely packet routing and this would allow for more even usage of memory buffers.

Conclusion

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,711,170 discloses a technique of bank balancing to provide for same level of occupancy among banks.

US Patent 6,842,826 discloses maintaining data blocks in a queue having a tail and a head end.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LK

Leonid Kravets
Patent Examiner
Art Unit 2189

November 22, 2005

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